REMARKS

Reconsideration and further examination of the application as amended are respectfully requested. All objections and rejections are respectfully traversed.

§112, Second Paragraph

Claims 1-9 and 11-18 were rejected under 35 U.S.C. §112, second paragraph, on the grounds that certain terms in claims 1, 12 and 16 lack antecedent basis. Applicants have amended claims 1, 12, 13 and 16 to provide a proper antecedent basis to the recited terms, and to correct several minor, typographical errors. Accordingly, Applicants request that the §112 rejection be withdrawn.

Applicants have also amended page 2 of the Specification to correct a minor, typographical error that was discovered. No new matter is being introduced.

§102

Claims 1-9 and 11-18 were rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 5,956,513 to Pawlowski ("Pawlowski"). Claims 1, 12 and 15 were additionally rejected under §102 as being anticipated by U.S. Patent No. 6,065,088 to Bronson et al. ("Bronson"). Applicants traverse the rejections for the reasons set forth below.

Claim 1, in relevant part, recites:

> "A method for preventing passive release of interrupts . . .",
>
> "forwarding an interrupt message . . . to the processor for servicing",
>
> "setting an interrupt pending flag",
>
> "in response to the interrupt being serviced, **generating a first ordered message**, the first ordered message notifying the subject I/O device that the interrupt has been serviced",

"**generating a second ordered message** for clearing the interrupt pending flag", and

"**sending the second ordered message** to the given port of the I/O bridge **after the first message has been sent**".

1. Pawlowski.

The Office Action cites to Col. 6, lines 40-41 of Pawlowski as disclosing Applicants claimed "generating a first ordered message" and their "sending the first ordered message to the given port of the I/O bridge". Applicants respectfully disagree that this excerpt or any portion of Pawlowski for that matter provides such a disclosure. In its entirety, this excerpt from Pawlowski states as follows:

> The [send pending] SP bit is reset when the [interrupt request register] IRR bit is set. The IRR bit is set when an interrupt message is accepted by the processor.

This excerpt makes no mention and provides no disclosure for the generation of any **ordered** message. Instead, what Pawlowski is describing is that the interrupt controller 34 of its host bridge 16 resets or clears the SP bit after setting the IRR bit, which the host bridge 16 does upon learning that the processor has accepted the interrupt message. None of the actions described by Pawlowski refer to any ordered messages. In fact, Pawlowski makes no disclosure at all of using or even supporting ordered messages. Accordingly, messages issued by Pawlowski's computer system may and likely will be delivered out of order. In contrast, claim 1 of Applicants' invention specifically recites "generating a first **ordered** message . . . notifying **the subject I/O device** that the interrupt has been serviced", and "generating **a second ordered message** for clearing the interrupt pending flag".

Because Pawlowski fails to disclose the generation and issuance of two ordered messages, among other deficiencies, the rejection of claim 1 based on this reference should be withdrawn. See MPEP §2131 (The identical invention must be shown in the cited reference in as complete detail as in the recited claim to support a rejection under §102).

2. Bronson.

Bronson too fails to anticipate the claimed invention.

As indicated above, claim 1 recites:

> "setting an interrupt pending flag in response to assertion of the interrupt signal",
>
> "in response to the interrupt being serviced, generating a first ordered message, the first ordered message notifying the subject I/O device that the interrupt has been serviced",
>
> "**generating a second ordered message for clearing the interrupt pending flag**",
>
> "deasserting the interrupt signal **in response to the first message**", and
>
> "clearing the interrupt pending flag in response to the second ordered message".

Among other things, Bronson fails to disclose the clearing of an interrupt pending flag in response to a second ordered message that is issued after the interrupt has been serviced. The Office Action equates Bronson's marking of its queue elements 104, 108 as "full", with the claimed setting of an interrupt pending flag. See Office Action at p. 7, citing to Col. 6, lines 38-41 of Bronson. Claim 1, however, goes on to recite that the claimed interrupt pending flag is cleared in response to the second ordered message, which is sent after the interrupt has been serviced. In contrast, Bronson clearly states that

his queue elements 104, 108 are marked "empty" once the respective interrupt is retrieved by the processor. See Bronson at Col. 6, lines 39-41 ("A queue element 104, 108 is marked empty (not full) when the interrupt contained in that queue element is taken by processor 80"). In other words, even assuming that Bronson's marking of his queue elements can be equated with Applicants' claimed setting and subsequent clearing of the interrupt pending flag, Bronson un-marks his queue elements 104 and 108 not with an ordered message, but simply upon transferring the interrupt to the processor for servicing. There is no disclosure by Bronson that his queue elements 104 and 108 are un-marked in response to any ordered message, and the Office Action cites to no such disclosure by Bronson.

Bronson also un-marks his queue elements 104 and 108 before the processor services the interrupt. That is, with Bronson, a queue element is un-marked as soon as the interrupt is transferred to the processor for servicing. There is no disclosure by Bronson of waiting to un-mark his queue elements until after the interrupt has been serviced, and no such disclosure is cited in the Office Action.

Because Bronson fails to disclose the clearing of an interrupt pending flag in response to an ordered message that is sent after the interrupt is serviced, the rejection based on Bronson should be withdrawn.

Claim 12, similarly, recites:

> "the interrupt controller, in response to assertion of an interrupt signal by a subject I/O device coupled to a given port of the I/O bridge, issues an interrupt message to the at least one processor and **sets an interrupt pending flag**",

"**the at least one processor**, upon servicing the interrupt, **sends first and second ordered messages** to the given port of the I/O bridge, the first ordered message notifying the subject I/O device that the interrupt has been serviced, and the second ordered message clearing the interrupt pending flag",

"the subject I/O device deasserts the interrupt signal in response to the first message", and

"the interrupt pending flag is cleared **in response to the second ordered message**".

As shown above, Pawlowski fails to disclose the issuance of any ordered messages by the processor. Bronson, moreover, fails to disclose the clearing of an interrupt pending flag in response to an ordered message issued after the interrupt is serviced. Accordingly, the rejection of claim 12 based on Pawlowski and Bronson should also be withdrawn.

Claims 2-9, 11 and 13-18 depend from allowable base claims. Accordingly, the rejection of these claims should also be withdrawn.

Applicants submit that the application, as amended, is in condition for allowance and early favorable action is respectfully requested.

Respectfully submitted,

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